

Appl. No. 09/995,319
Amdt. Dated November 9, 2005
Reply to Office Action of August 9, 2005

Attorney Docket No. 81784.0246
Customer No. 26021

REMARKS/ARGUMENTS

Claims 1-12 and 16-20 are pending in the Application. Reconsideration and allowance in view of the following remarks are respectfully requested.

In Paragraph 3 which begins on page 2 of the Office Action, claims 1-12 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,552,324 of Kothari et al. In Paragraph 5 which begins on page 4 of the Office Action, claims 16-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kothari et al. in view of U.S. Patent 6,686,957 of Johnson et al. These rejections are respectfully traversed.

The present invention relates to a source follower amplification circuit wherein an amplification transistor, a load transistor, and a control transistor are connected between a first power source and a second power source. In the source follower amplification circuit of the present invention, a current flows from the first power source to the second power source.

In contrast, Kothari et al. does not describe a source follower amplification circuit. According to the Office Action, the first power source of the present invention corresponds to VDD2 of Kothari et al., and the second power source of the present invention corresponds to VDD1 of Kothari et al. It is further indicated in the Office Action that the amplification transistor, the load transistor and the control transistor respectively correspond to "M1A, M1B, M2A, M2B", "M3 or M4", and "M9A or M9B or M6A or M7A" of Kothari et al. However in Kothari et al., no current flows from VDD2 to VDD1.

In the case of Johnson et al., this reference does not describe or suggest a structure relating to a source follower amplification circuit in the manner of the present invention.

Claims 1-12 and 16-20 are submitted to clearly distinguish patentably over the cited references in their present form. In the case of claim 1, for example, such

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Claim defines a "source follower amplification circuit" which includes "an amplification transistor", "a load transistor coupled between the amplification transistor and a first power source" and "a control transistor connected between the amplification transistor and a second power source". In accordance with the invention, claim 1 includes "an output control circuit, connected to a gate of the control transistor, for outputting the control signal for reducing a current flowing from the second power source to the amplification transistor during a period in which a pixel signal is not read". Therefore, claim 1 clearly distinguishes patentably over the cited art.

Claims 2-6 depend directly or indirectly from and contain all of the limitations of claim 1 so as to also distinguish patentably over the cited art.

Claim 7 defines a "source follower amplification circuit" in terms of limitations similar to claim 1. Therefore, such claim is also submitted to clearly distinguish patentably over the art.

Claims 8-12, 16 and 17 depend, directly or indirectly, from claim 7 and contain all of the limitations thereof, so that such claims are also submitted to clearly distinguish patentably over the art.

Claim 18 depends from and contains all of the limitations of claim 1, so that such claim is submitted to clearly distinguish patentably over the art.

Independent claims 19 and 20 define "a source follower amplification circuit" in terms of limitations similar to those of claim 1, so that such claims are also submitted to clearly distinguish patentably over the art.

In conclusion claims 1-12 and 16-20 are submitted to clearly distinguish patentably over the cited art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los

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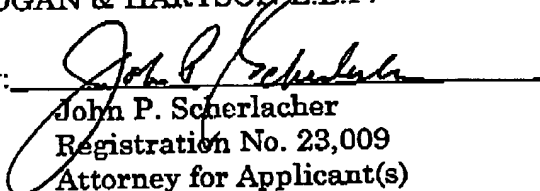
Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: November 9, 2005

By: _____


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